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10/579,542	02/28/2007	Ewald Gunther	E3311.0005.	8458
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EXAMINER				
CHU, CHRIS C				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/579,542

**Applicant(s)**

GUNTHER ET AL.

**Examiner**

CHRIS C. CHU

**Art Unit**

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 14 - 32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14 - 32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 May 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SI/300)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_
- Paper No(s)/Mail Date 7/9/08 and 8/17/06

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "5" and "6" have both been used to designate the edge surrounding layer or insulating layer or planar conducting structure. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

2. Claim 15 is objected to under 37 CFR 1.75(c) as being in improper form because a dependent claim 15 is depending to a cancelled claim 1. See MPEP § 608.01(n). For the purpose of the examination, the examiner treated the claim 15 as a dependent claim to the independent claim 14.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 14 – 21, 23 – 25 and 27 – 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto et al. (U. S. Pat. No. 6,404,792).

Regarding claim 14, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 an article of manufacture (the article in e.g., Fig. 4 and Fig. 30) comprising:

- a substrate (35; column 6, lines 45 and 46) ; and
- an optoelectronic component (11; column 5, lines 2 – 3),
- wherein the optoelectronic component (11) is contacted in a planar manner (see e.g., Fig. 4).

Regarding claim 15, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the substrate (35) having a conducting element (36 or/and 37; column 6, line 46) with which the optoelectronic element (11) is contacted in a planar manner (see e.g., Fig. 4 and Fig. 30).

Regarding claim 16, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the conducting element (36 or/and 37) being a printed conductor (column 6, line 46).

Furthermore, the limitation “printed” is product-by-process limitation. Even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A “product by

process” claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**; In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**; In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a “product by, all of” claim, and not the patentability of the process, and that an old or obvious product, whether claimed in “product by process” claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 17, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the substrate (35) and/or the optoelectronic component (11) being at least partially provided with an insulating layer (40; column 6, line 19), on which a planar conducting structure (41 or/and 42; column 6, line 52) is disposed for planar contacting of the optoelectronic component (11; see e.g., Fig. 4 and Fig. 30).

Regarding claim 18, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the insulating layer (40) comprising one or more of a foil, enamel, and a polymer layer (column 6, line 19).

Regarding claim 19, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the insulating layer (40) being transparent in the area (column 7, lines 4 – 7) of a light exit and/or entry opening of the optoelectronic component (11; see e.g., Fig. 4 and Fig. 30).

Regarding claim 20, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 a window (the opening area for the element 32 or 31) being opened in the insulating layer (40) in the area of a light exit and/or entry opening of the optoelectronic component (11; see e.g., Fig. 4 and Fig. 30).

Regarding claim 21, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 in the insulating layer (40) in the area of a contact point (the attached area between the elements 42 and 32) for the optoelectronic component (11) a window (the opening area for the element 32 or 31) being opened through which the planar conducting structure (42 and/or 41) is led to the contact point of the optoelectronic component (11; see e.g., Fig. 4 and Fig. 30).

Regarding claim 23, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the planar contact at least partially covering a light exit and/or entry opening (the opening area for the light exit and/or entry, e.g., 33) of the optoelectronic component (11; see e.g., Fig. 4 and Fig. 30).

Regarding claim 24, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the optoelectronic component (11) comprising one or more of an LED (column 5, lines 2 – 3), an OLED, and a photovoltaic component.

Regarding claim 25, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the substrate (35) being one of: a printed circuit board, a Flex, and a lead frame (column 1, lines 58 – 59).

Regarding claim 27, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 a method of making an article (the article in e.g., Fig. 4 and Fig. 30) of manufacture comprising a substrate (35) and an optoelectronic component (11), the method comprising contacting the optoelectronic component (11) in a planar manner (11; see e.g., Fig. 4 and Fig. 30).

Regarding claim 28, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 an article of manufacture (the article in e.g., Fig. 4 and Fig. 30) comprising:

- a substrate (11) having a substrate contact (36 and/or 37);
- an optoelectronic component (11), said optoelectronic component (11) having a central light exit (column 6, lines 56 – 59) and an edge contact (32 and/or 31)

- disposed at least partially around a periphery of the light exit (see e.g., Fig. 4 and Fig. 30); and
- a conducting structure (42 and/or 41), arranged on the optoelectronic component (11) and the substrate (35) so as to contact the edge contact (32 and/or 31) and the substrate contact (36 and/or 37; see e.g., Fig. 4 and Fig. 30).

Regarding claim 29, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 an electrically insulating layer (40) contacting the optoelectronic component (11), on which the planar conducting structure (42 and/or 41) is disposed (see e.g., Fig. 4 and Fig. 30).

Regarding claim 30, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the electrically insulating layer (40) having a window (the opening area for the element 32 or 31) formed in an area of the light exit (see e.g., Fig. 4 and Fig. 30).

Regarding claim 31, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the electrically insulating layer (40) having transparent portion (column 7, lines 4 – 7) formed in an area of the light exit (column 6, lines 56 – 59 and see e.g., Fig. 4 and Fig. 30).

Regarding claim 32, Yamamoto et al. discloses in e.g., Fig. 4 and Fig. 30 the conducting structure (42 and/or 41) being a metallic layer (column 7, lines 20 – 22).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. in view of Tanabe et al. (U. S. Pat. No. 6,479,930).

While Yamamoto et al. discloses the use of the insulating layer, Yamamoto et al. does not disclose the insulating layer containing pigments to color the light emitted from or absorbed by the optoelectronic component. Tanabe et al. teaches an insulating layer (3; column 1, line 60) containing pigments to color the light emitted from (column 1, lines 58 – 65) or absorbed by an optoelectronic component (the EL element; column 1, lines 6 and 7). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the pigments of Tanabe et al. into the insulating layer of Yamamoto et al. as taught by Tanabe et al. to convert a color other than the intrinsic color of the layer (column 1, lines 61 – 62).

7. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. in view of Katoh (U. S. Pat. No. 7,126,163).

While Yamamoto et al. discloses the use of the article of manufacture, Yamamoto et al. does not disclose the height of the article of manufacture being less than 0.4 mm. Katoh teaches a height of the article of manufacture (the LED; column 7, lines 23 – 25) being less than 0.4 mm (column 7, lines 23 – 25). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the height of Katoh to be the specific height of the article of manufacture of Yamamoto et al. as taught by Katoh to provide a thinner-sized LED (column 7, lines 28 – 30).

### ***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's



disclosure. Härle et al., Okazaki, Cole, Katsuno et al., Nagai, Kameyama et al., Nishi et al., Nagai et al., Ouchi et al., and Furukawa et al. disclose a LED device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRIS C. CHU whose telephone number is (571)272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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